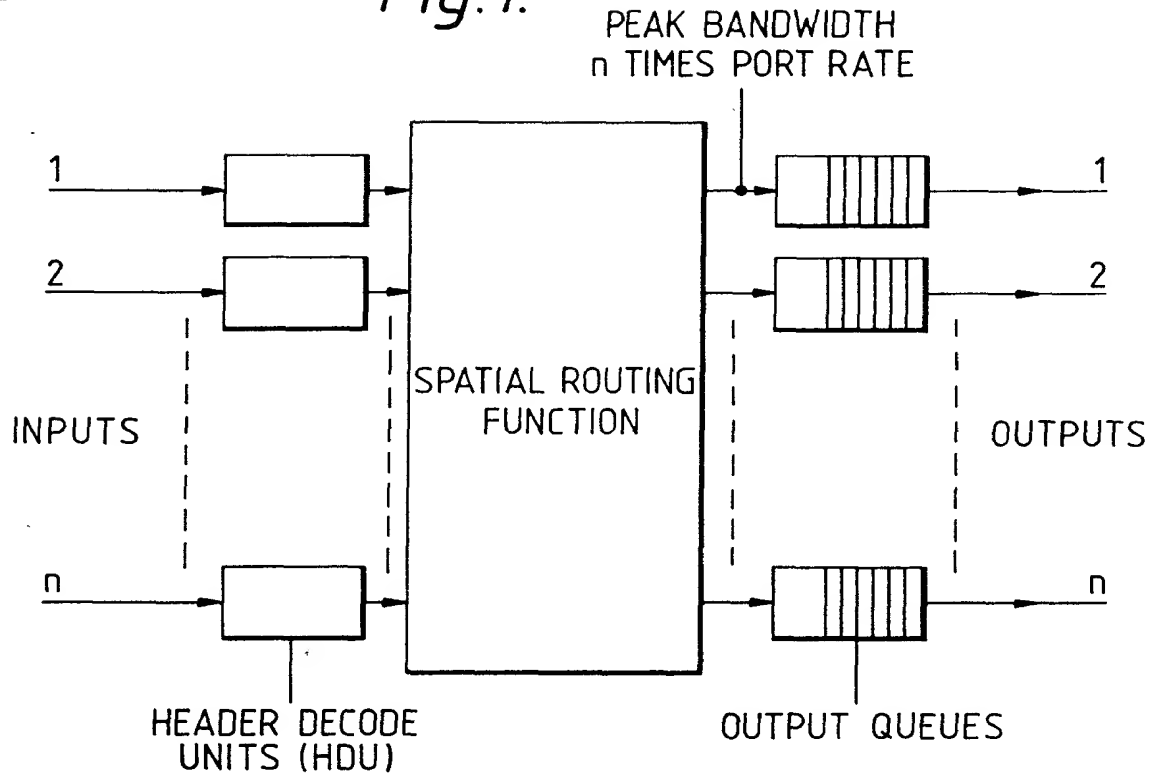


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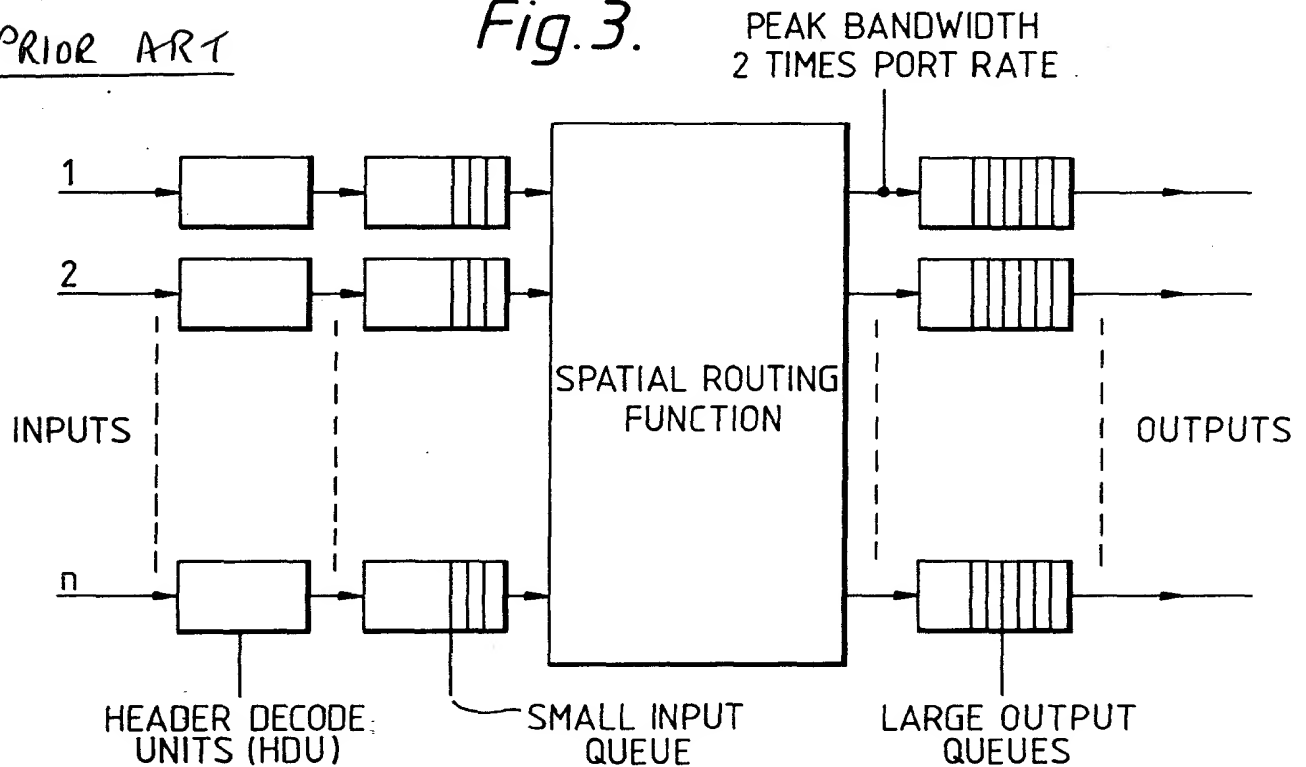
Prior Art

Fig. 1.



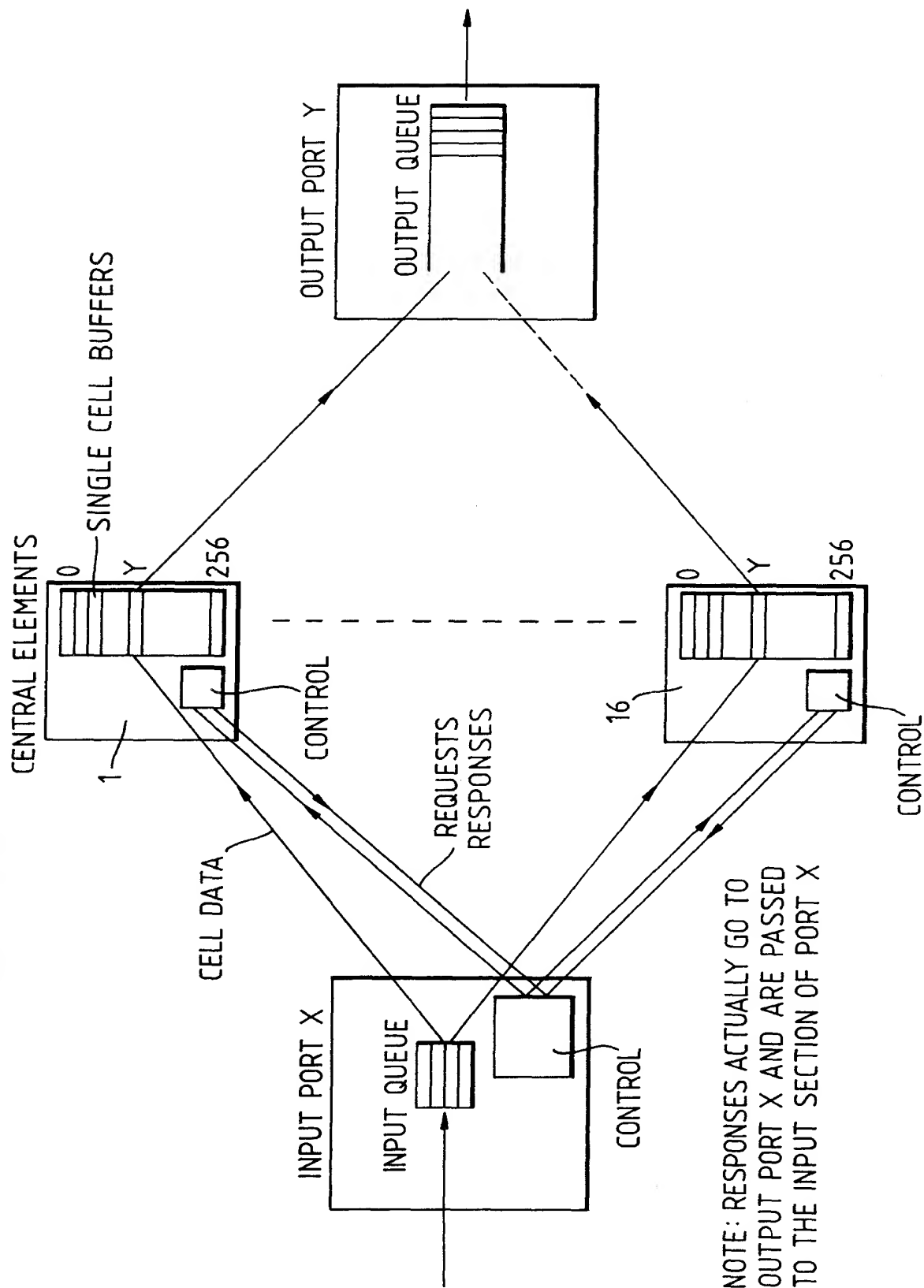
Prior Art

Fig. 3.



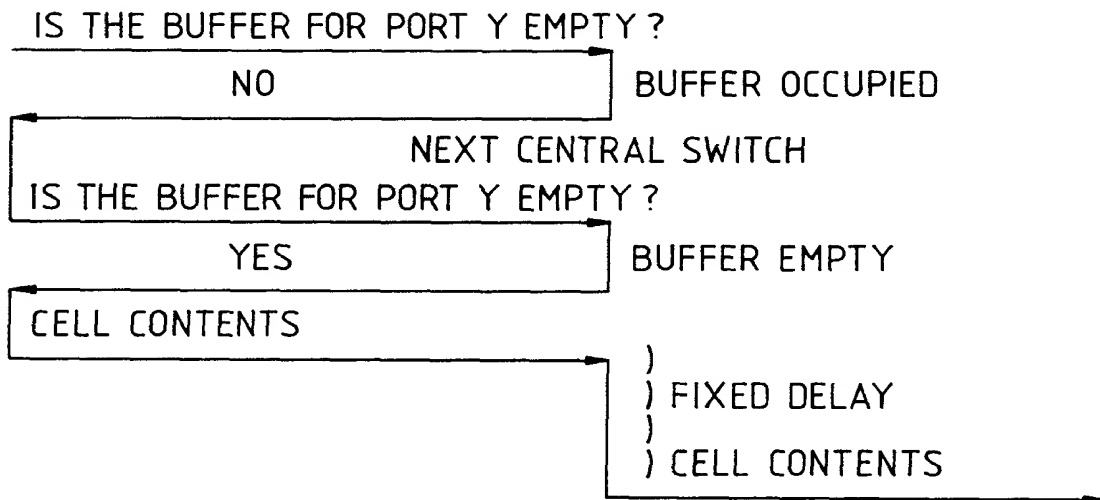
PRIOR ART

Fig. 2.



PORT X

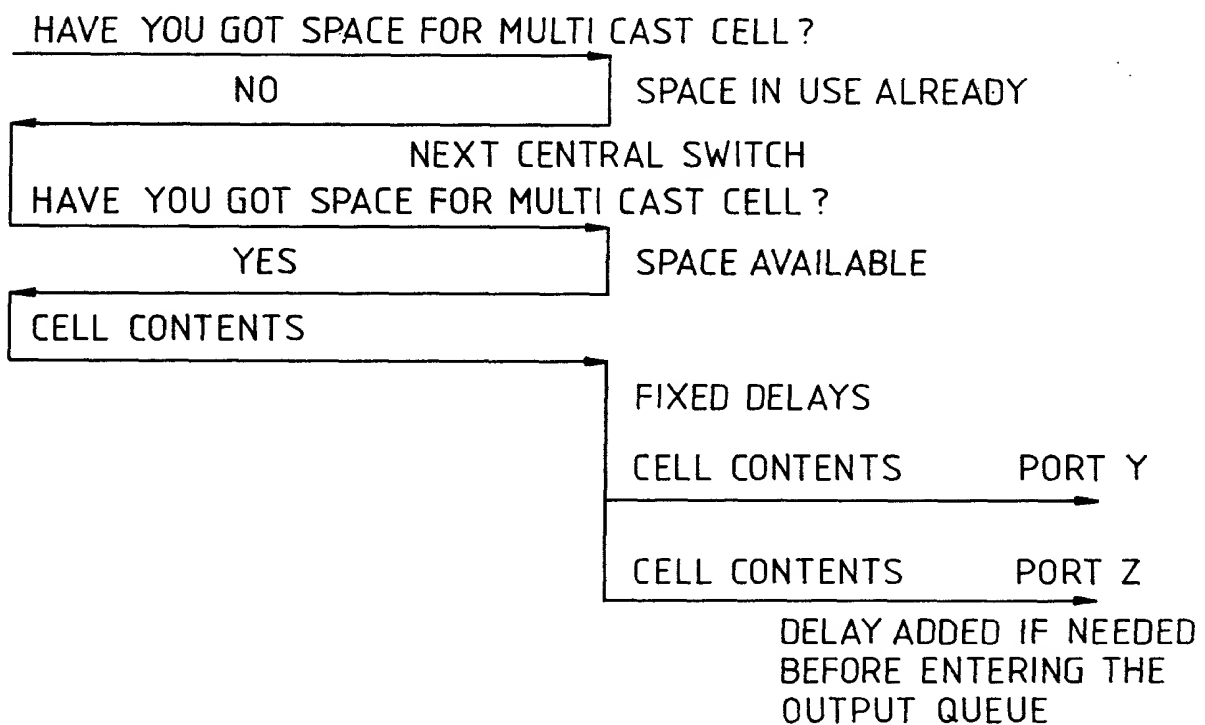
PORT Y



PRIOR ART

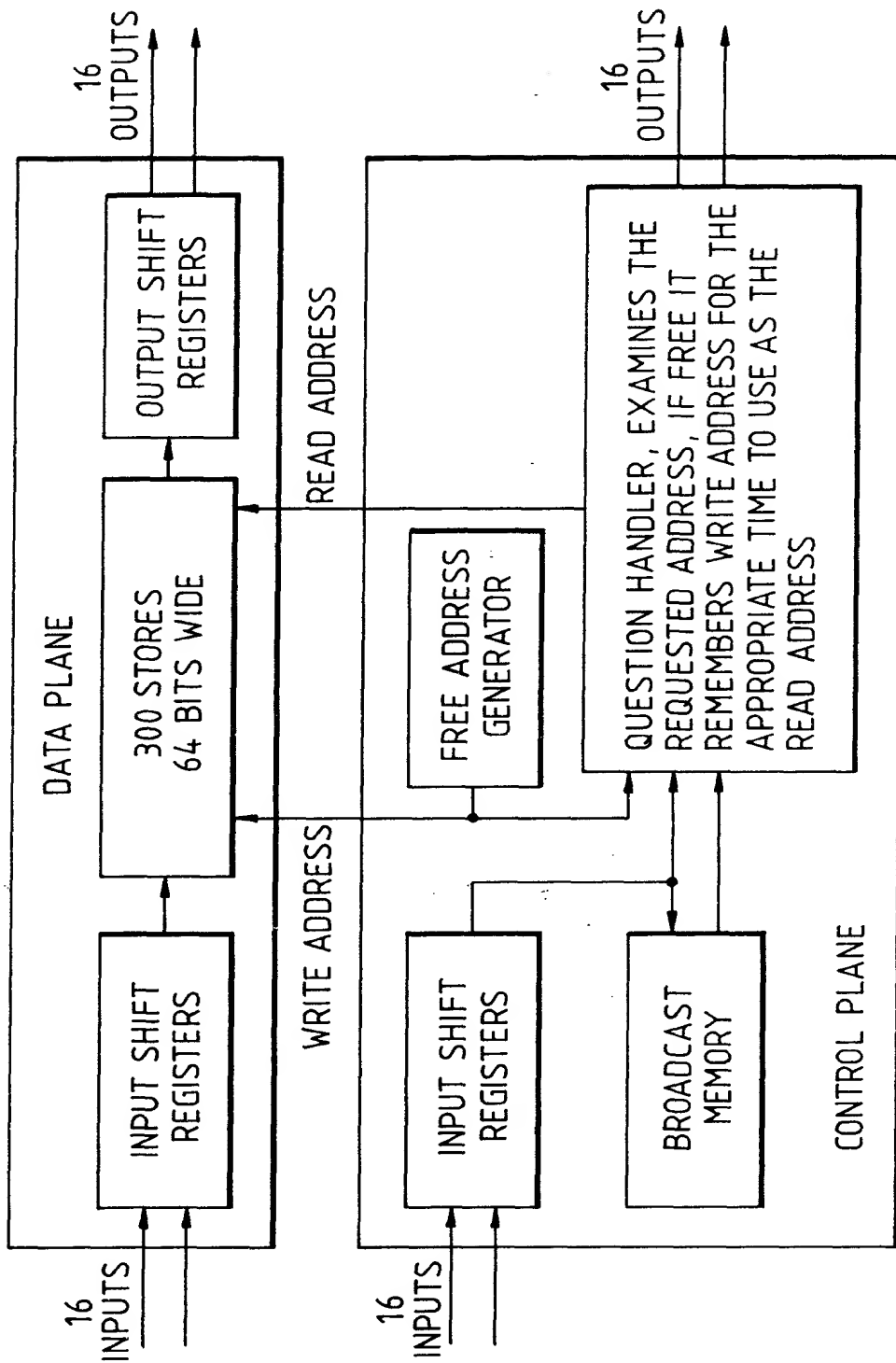
PORT X

PORT Y



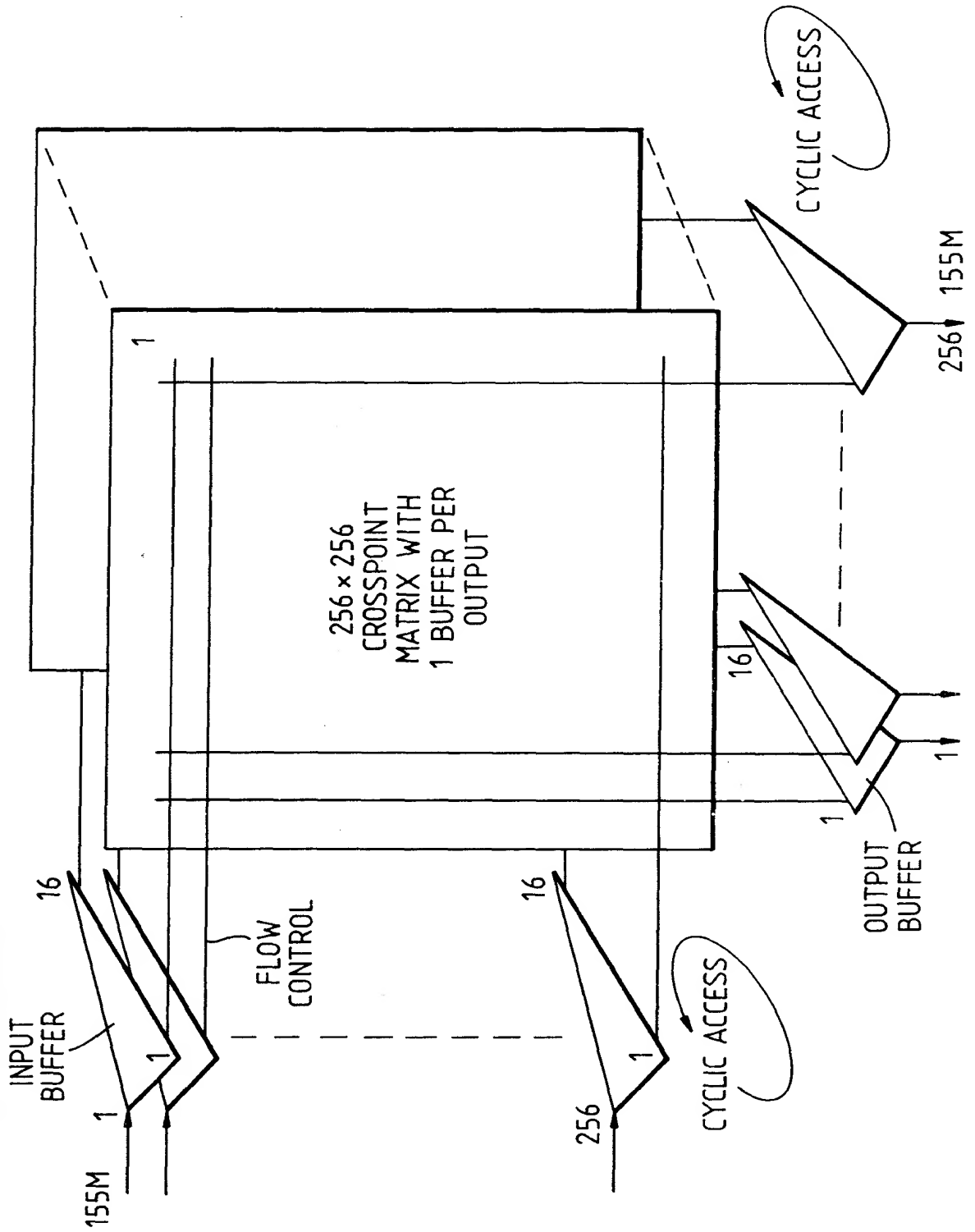
PRIOR ART

Fig. 6.



PRIOR ART

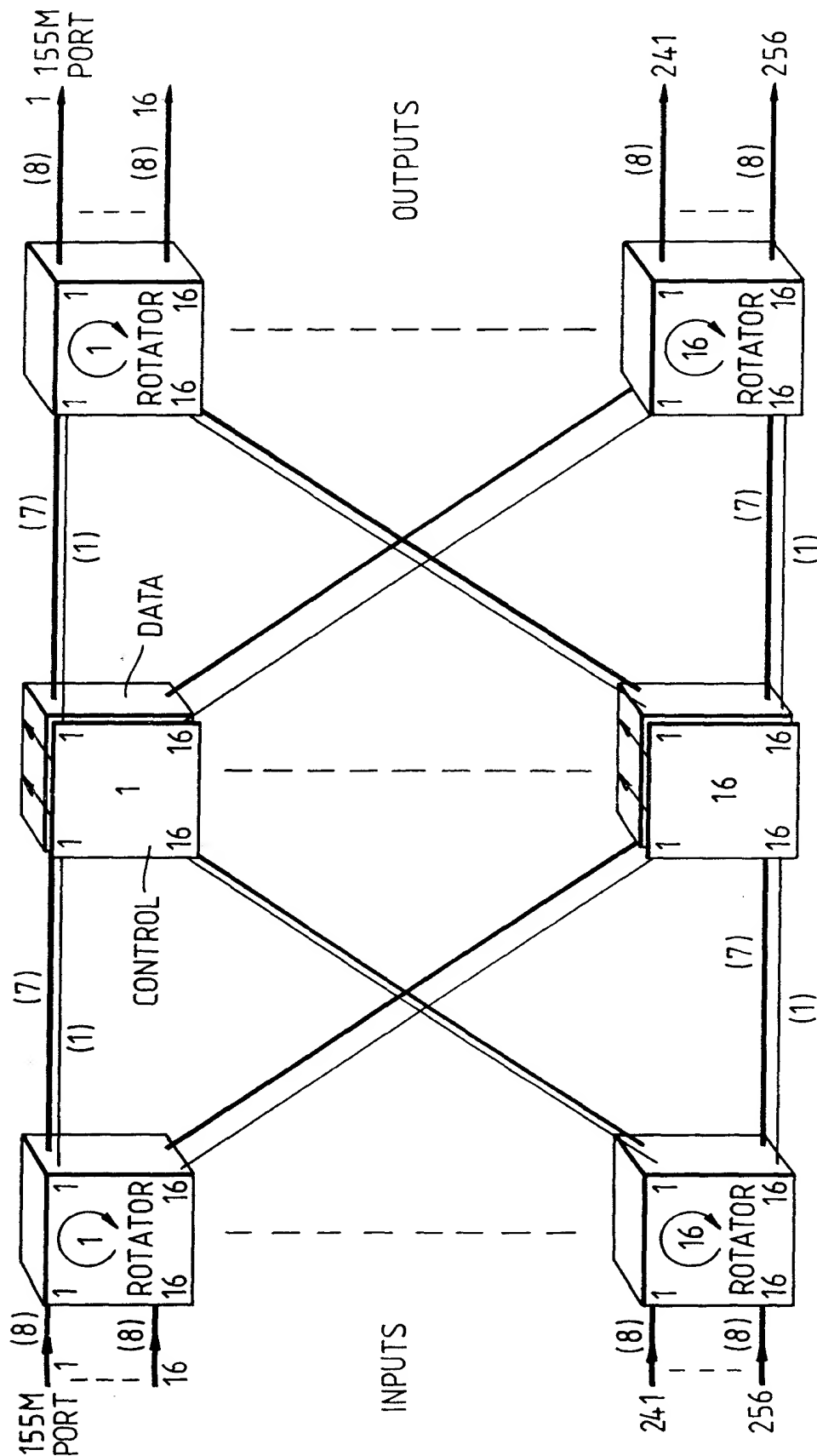
Fig. 7.



Prior Art

Fig. 8.

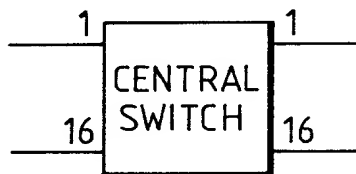
NOTE : ANY NUMBER OF INPUT /OUTPUT "PORTS" CAN BE CONCATENATED WITH GUARANTEED CELL SEQUENCE INTEGRITY TO ALLOW EVOLUTION TO 600M, 2.4G, 9.6G ETC.



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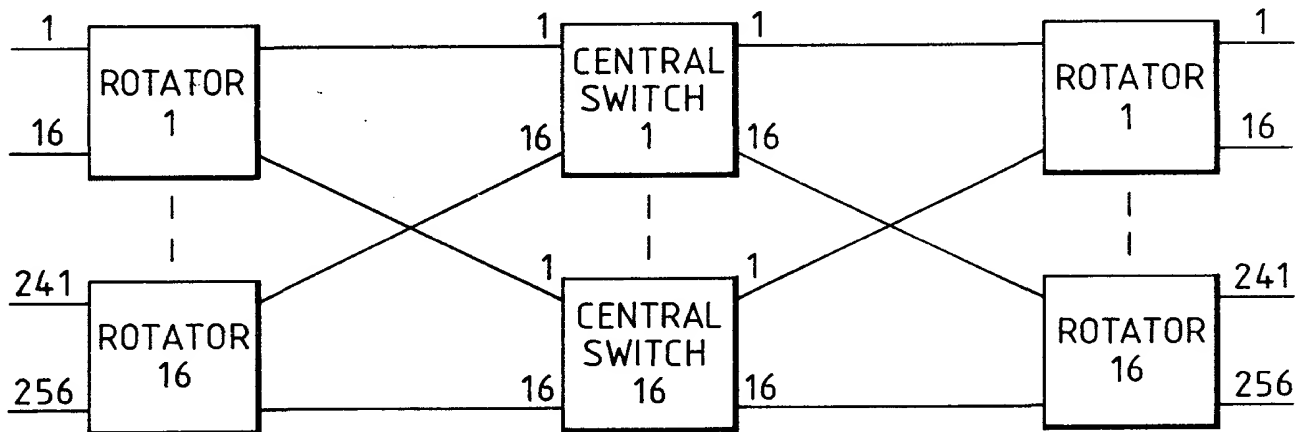
PRIOR ART

Fig. 10a.



PRIOR ART

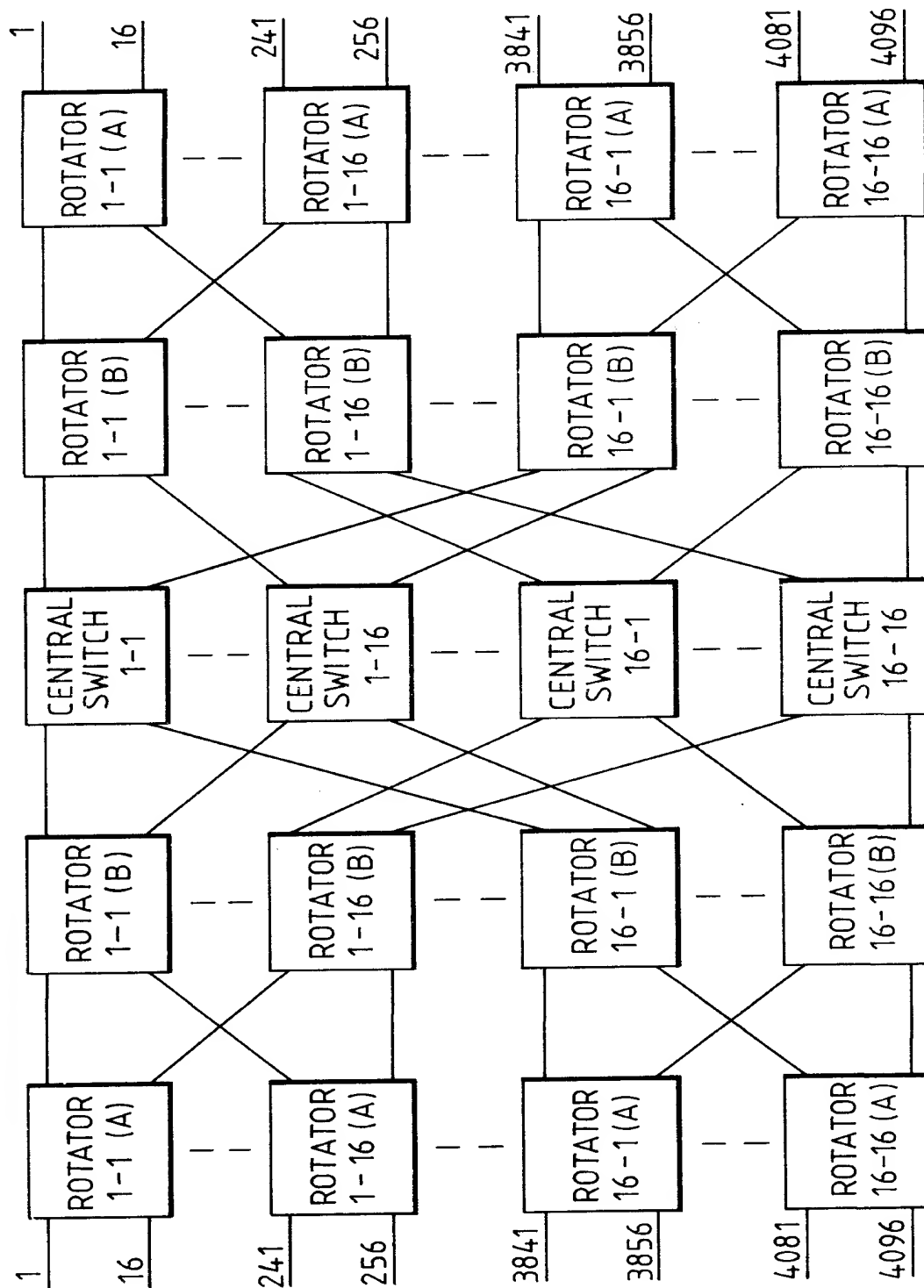
Fig. 10b.



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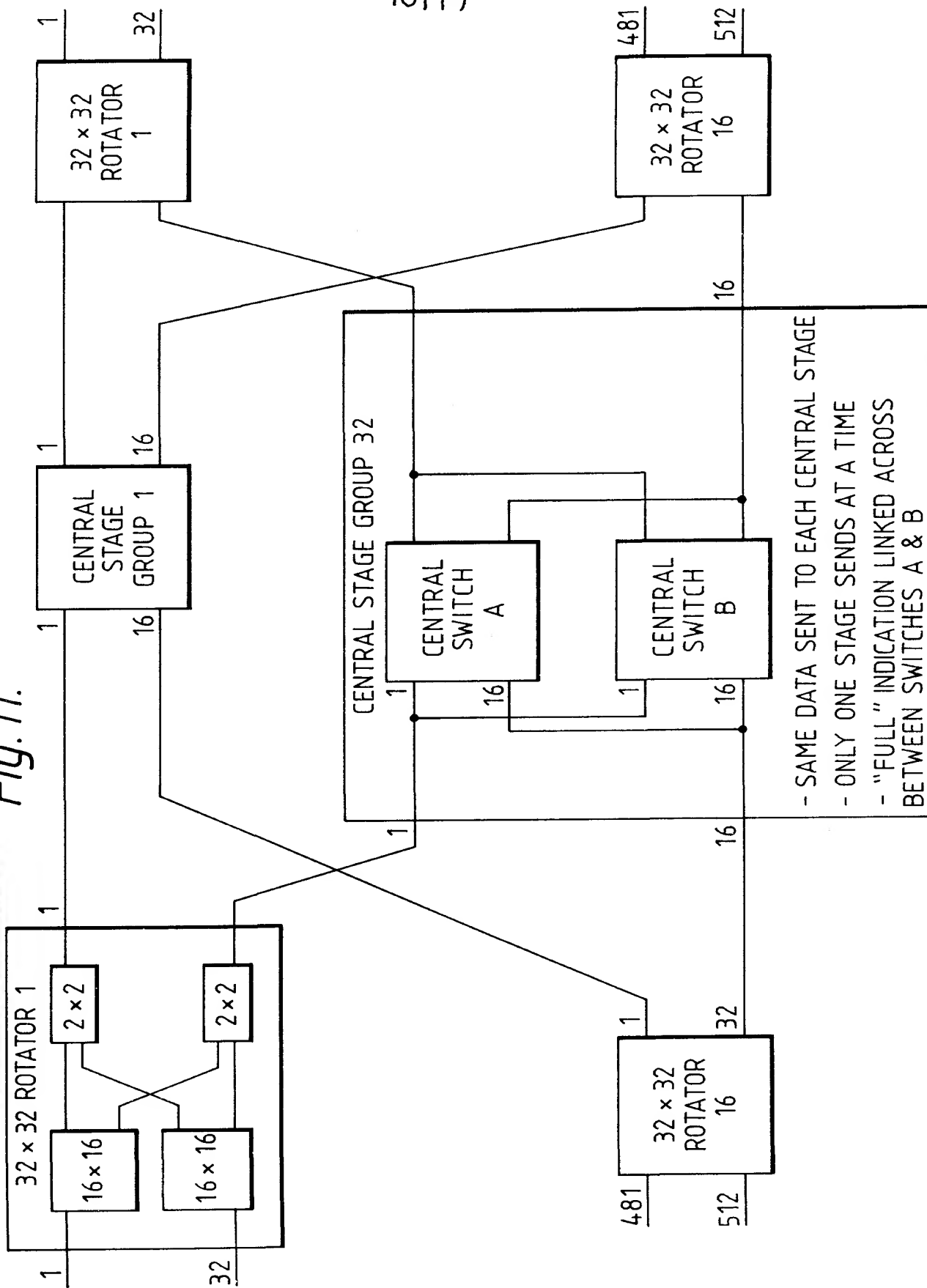
Fig. 10c.

PRIOR ART



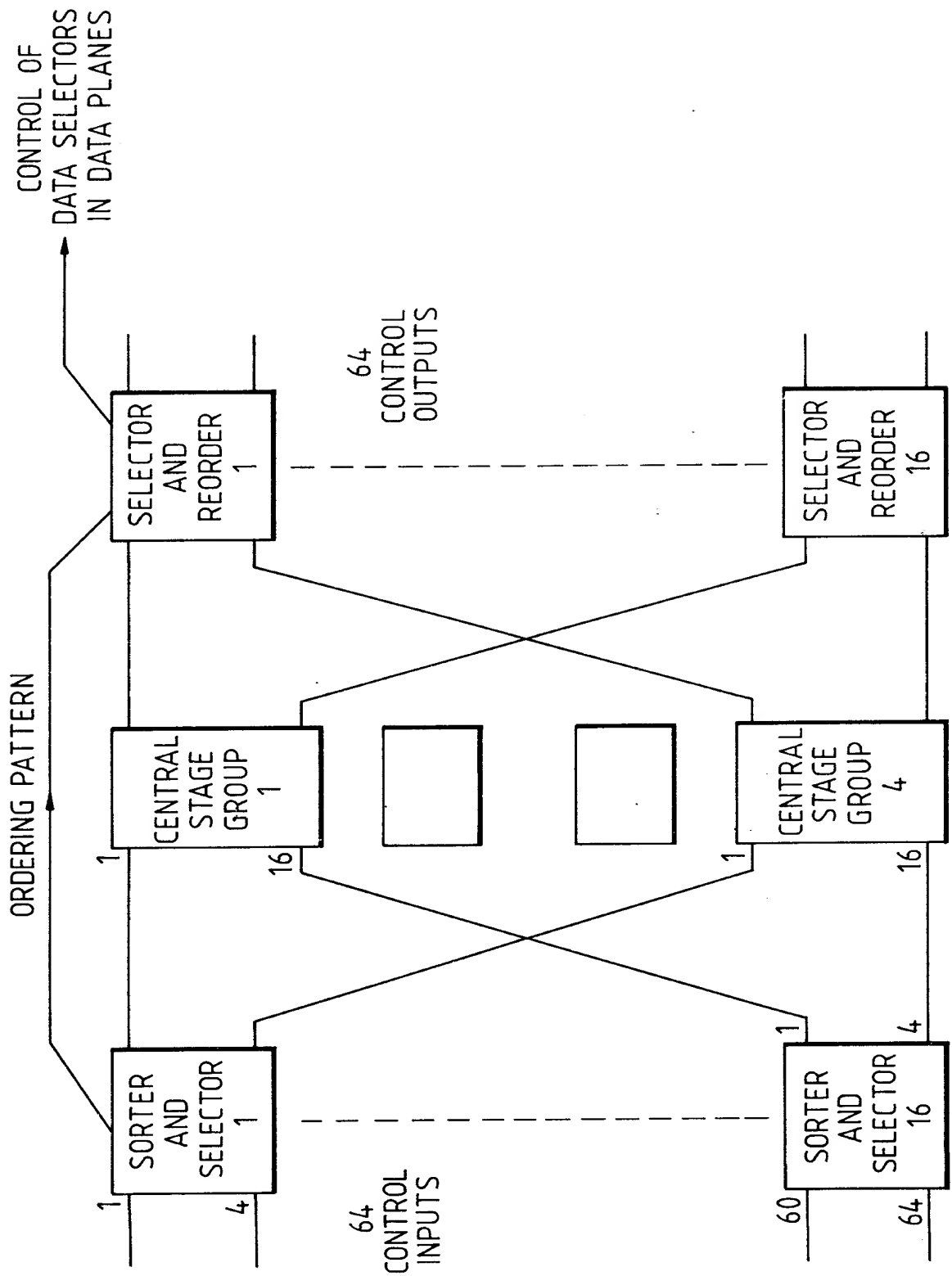
PRIOR ART

Fig. 11.



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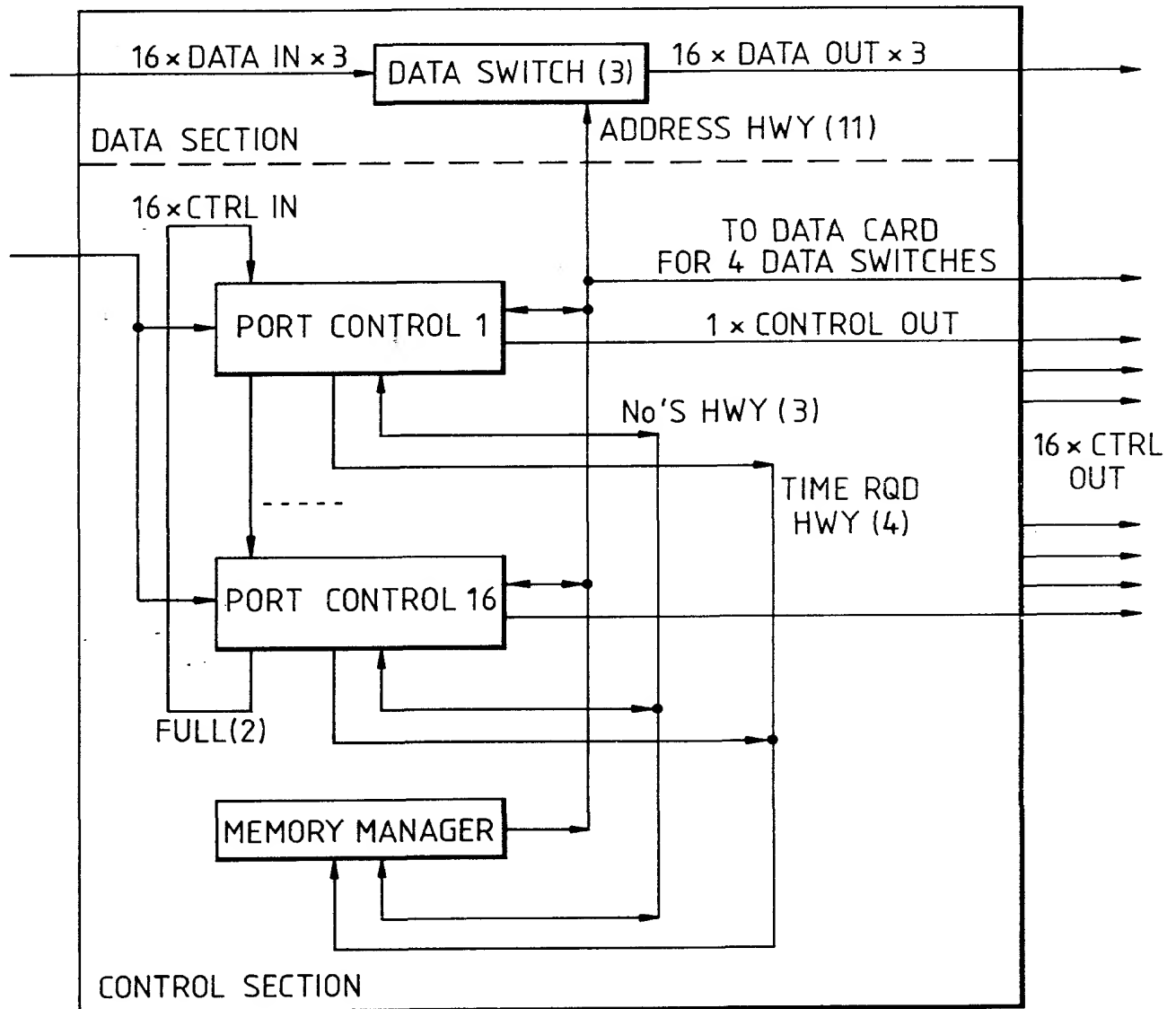
PRIOR ART Fig. 12.



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PRIOR ART

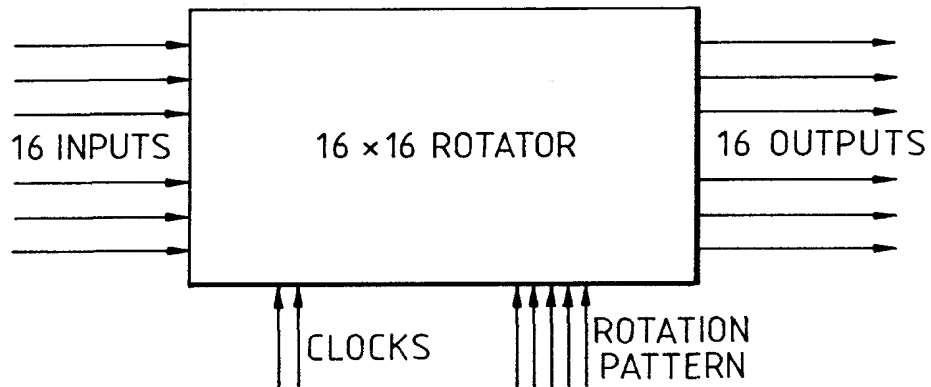
Fig. 13.



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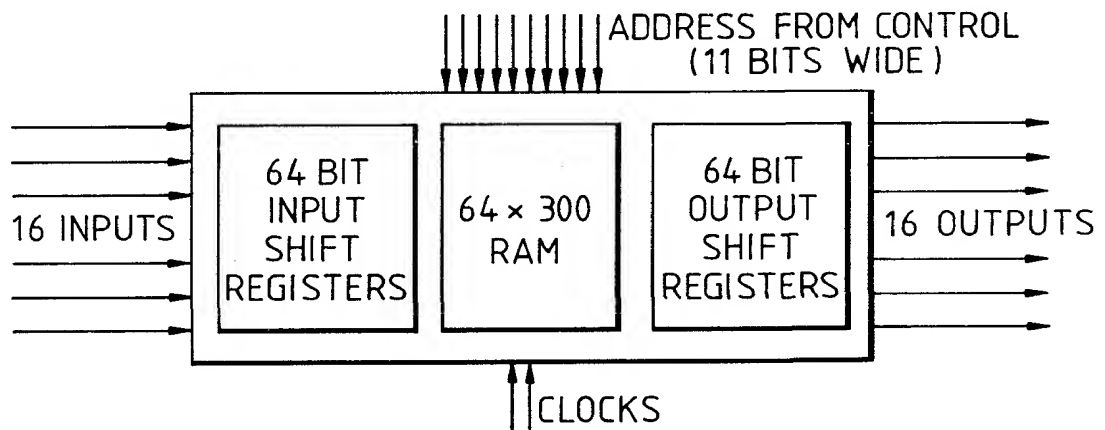
PRIOR ART

Fig. 14.



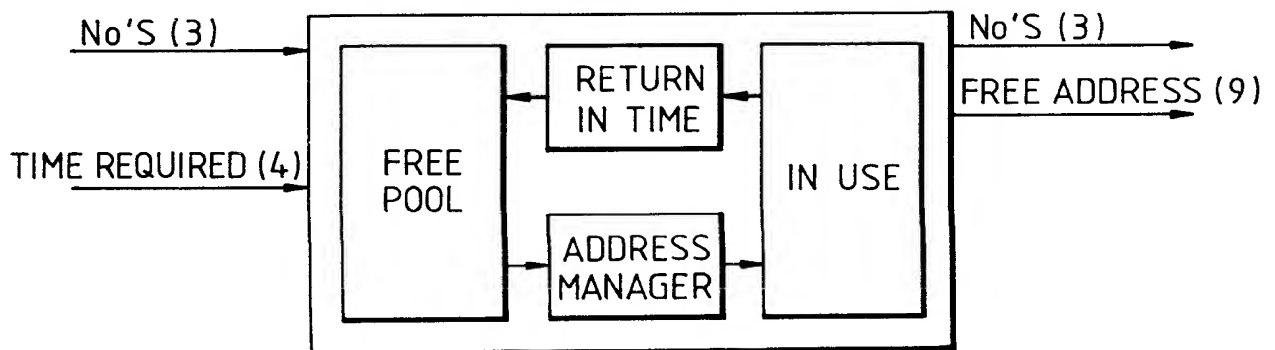
PRIOR ART

Fig. 15.



PRIOR ART

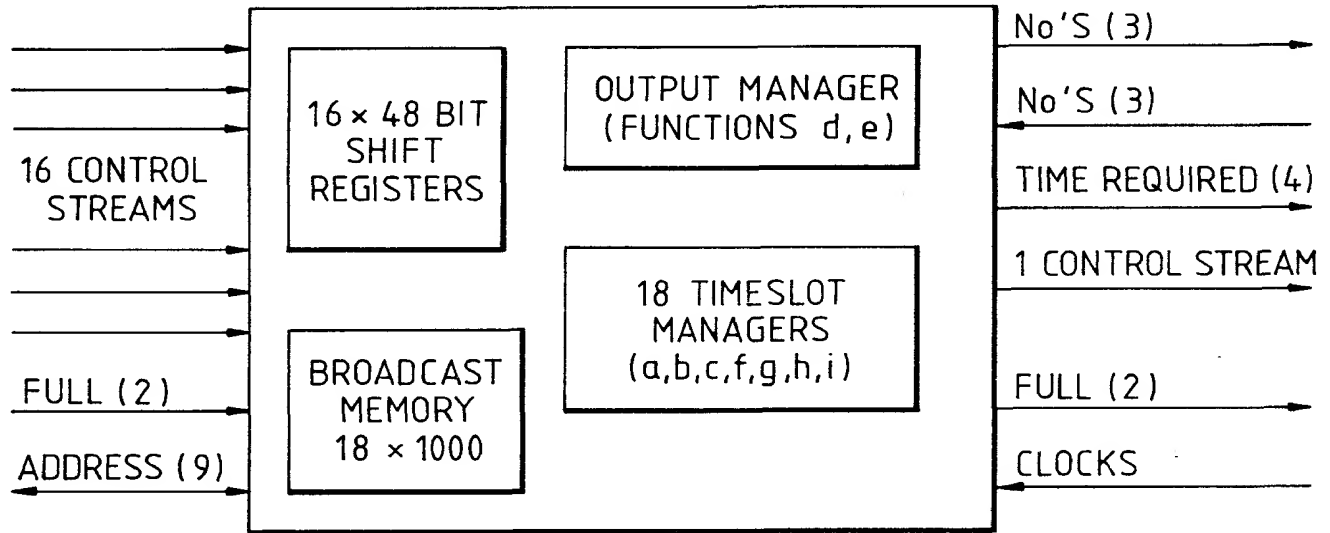
Fig. 16.



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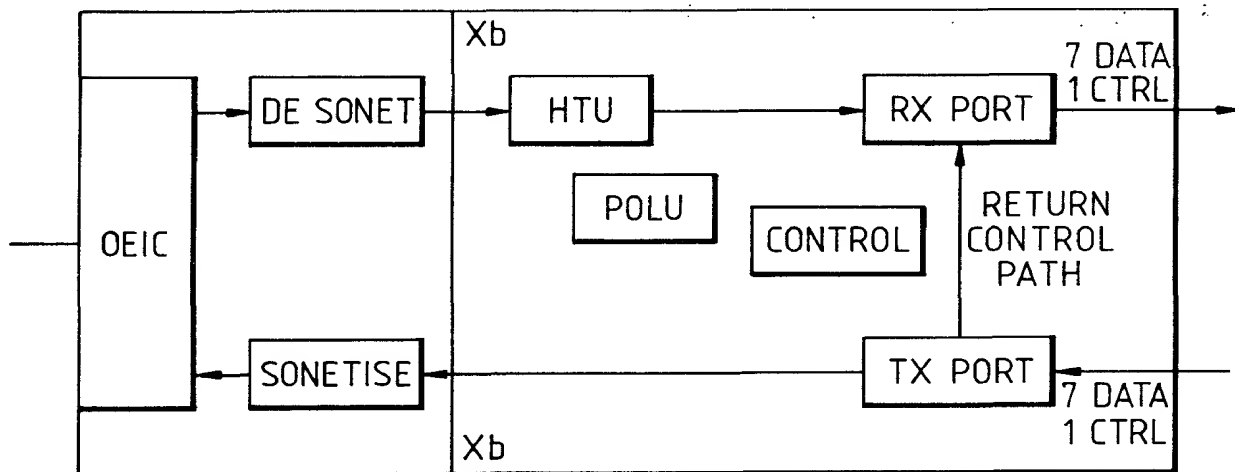
PRIOR ART

Fig. 17.



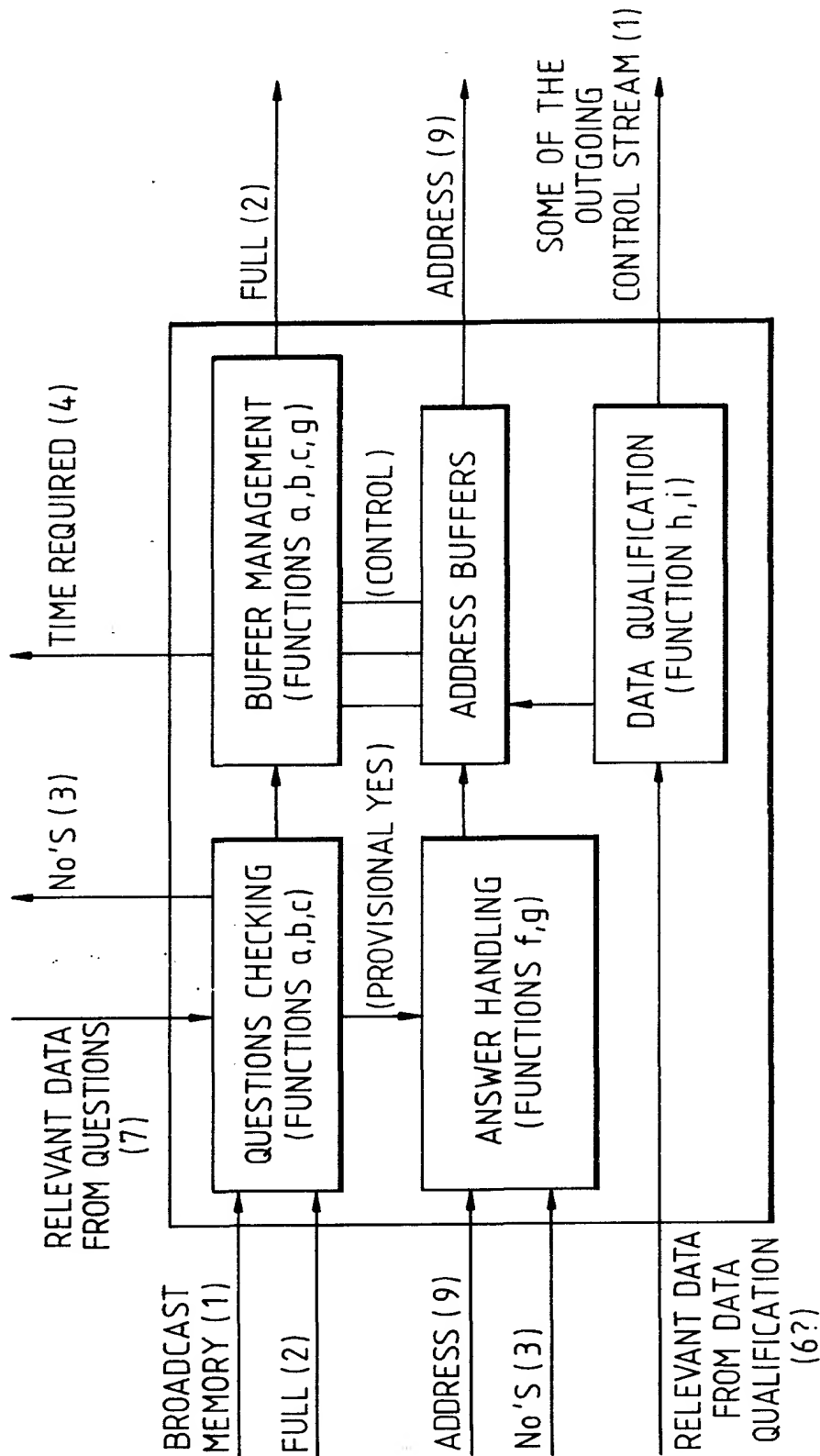
PRIOR ART

Fig. 19.



PRIOR ART

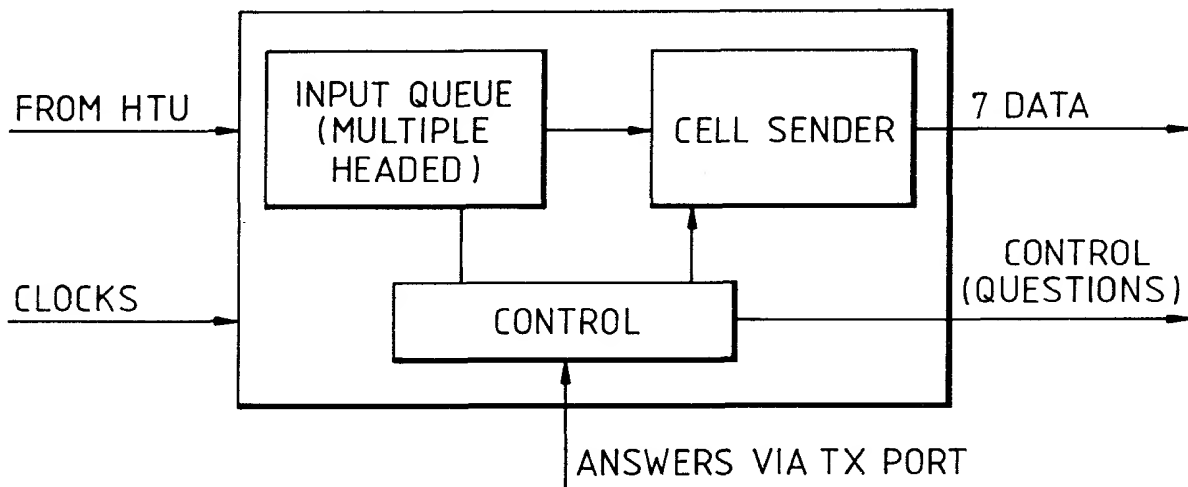
Fig. 18.



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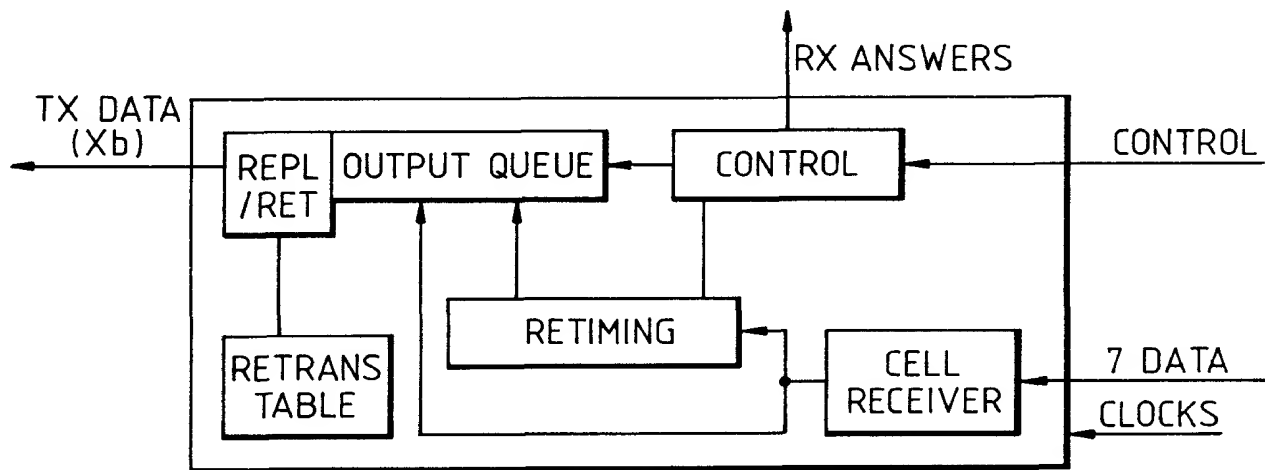
PRIOR ART

Fig. 20.

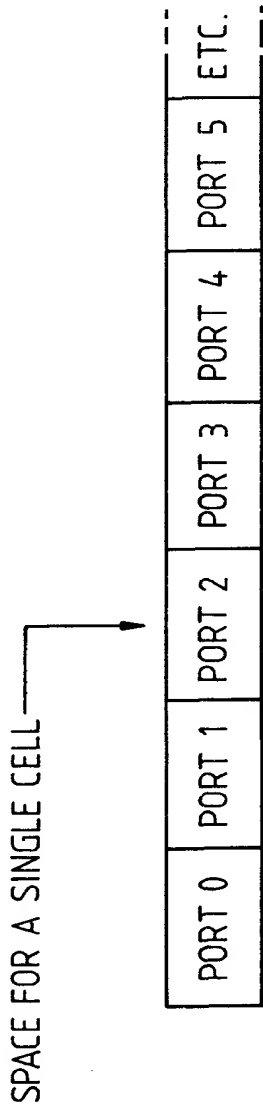


PRIOR ART

Fig. 21.



Prior Art Fig. 22A.



SINGLE CELL STORAGE, FOR POINT TO POINT CELLS

Prior Art Fig. 22B.

FORWARD TRANSFER SPACE							TOP RANK
							MID RANK(S)
AS ABOVE	PORT 0	PORT 1	PORT 2	PORT 3	PORT 4	PORT 5	MAIN RANK

ADDITIONAL STORAGE FOR MULTIPOINT CELLS

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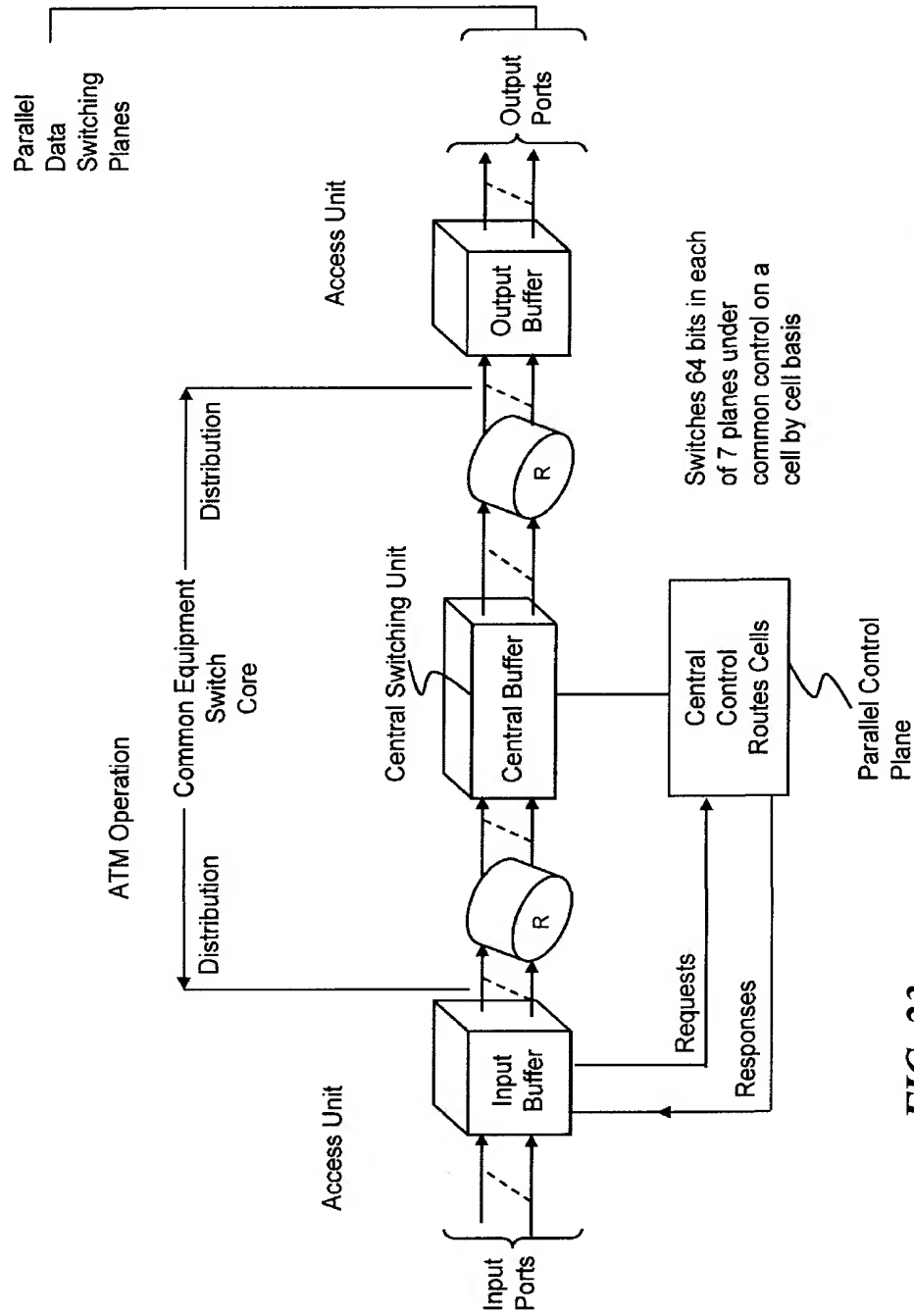


FIG. 23

PRIOR ART

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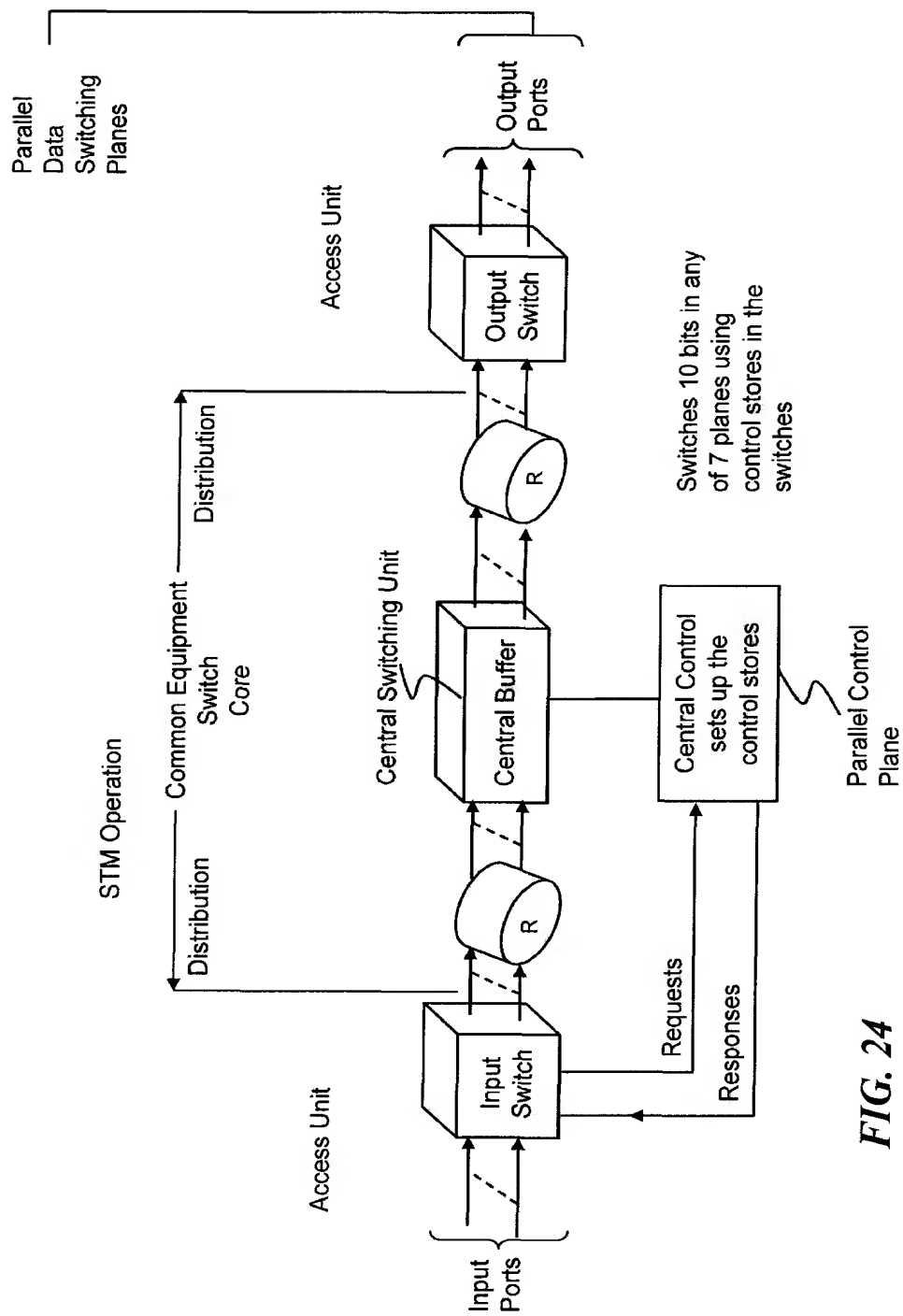


FIG. 24